NDC100S

5.25 INCH Winchester Disk Drive Controller

—SCSI—

National Computer Ltd.

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CONTENTS

DESCRIPTION

The NDC100S Disk Drive Controller controls the operation of up to two 5¼ inch Winchester disk drives with an interface compatible with the interface of Seagate Technology's ST506. NDC100S is designed on a compact printed circuit board and can be easily mounted on a 5¼ inch disk drive. Since the controller uses the Small Computer System Interface, it can communicate with popular host buses without any special designs.

1. GENERAL SPECIFICATIONS

1.1 Disk Interface

ST506 disk drive interface compatible

1.2 Host Interface

SCSI (Small Computer System Interface)

1.3 Control Functions

Disk drives:	2 max.
Heads:	8 max.
Logical sectors:	1 FFFFFH max. (less than FFFFH in converted into physical cylinders)
Sector length:	128 B/256 B/512 B/1024 B
Data buffer:	full-sector buffer
Multi-sector:	256 sectors max.
Erros check:	ECC 11 bit burst correction
Over-lapped seek:	in buffer mode

1.4 Hardware Specification (in Block Diagram)

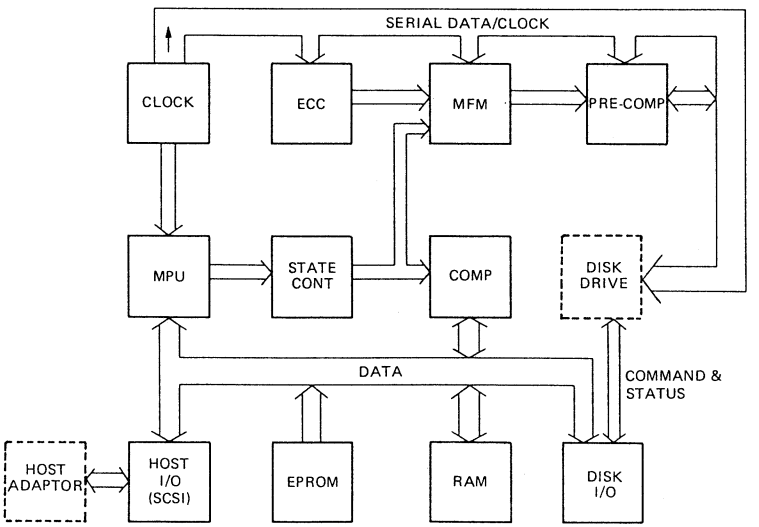


Figure 1

1.5 Board Dimensions

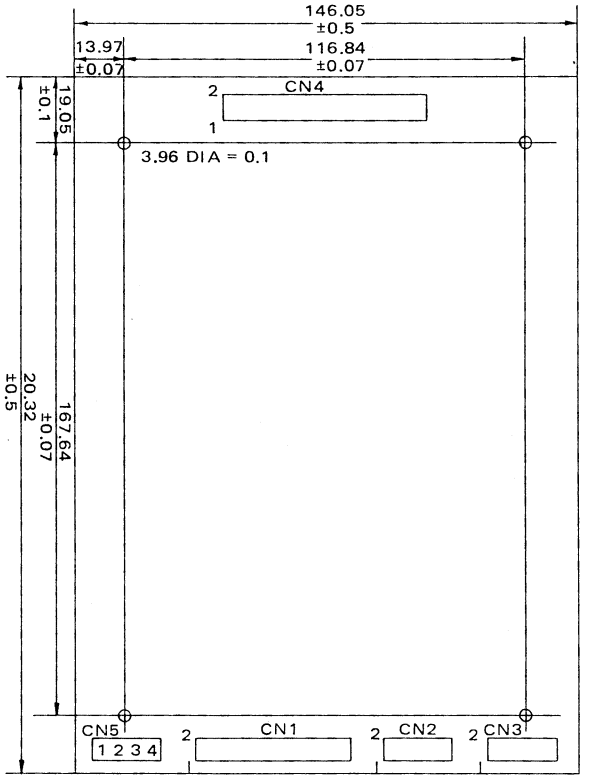


Figure 2

1.6 Connectors

Destination	Function	Type
CN1	Drive control signals	JAE PS-34PA-D4T1-A1
CN2, 3	Drive data signals	JAE PS-20PA-D4T1-A1
CN5	Power supply	AMP 1-480424-0 (housing) AMP 350078-4 (pins)
CN4	Host interface signals	JAE PS-50PA-D4T1-A1

JAE: Japan Air Electronics

1.7 Voltage Source and Environmental Conditions (controller section)

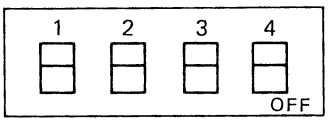
- +5 V DC, 1.8 A (max.)
- Temperature: 0°C ~ 50°C
- Humidity: 10% ~ 80% RH

2. SET-UP

Before the controller can be operated, the dip-switches (SW1) and mumper plugs (JP1) must be selected.

2.1 Dip-Switches (SW1)

Dip-switches (SW1) specify the sector lengths as follows.



SW1

Figure 3

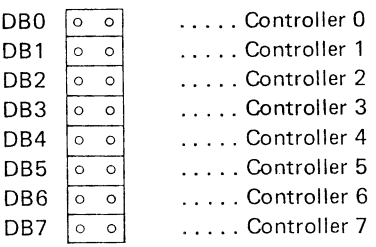
ON	OFF	LENGTH
1	2, 3, 4	128B
2	1, 3, 4	256B
3	1, 2, 4	512B
4	1, 2, 3	1024B

Table 1

NOTE: When all switches are off, the controller can not operates.

2.2 Jumper Plug (JP1) (Multiple controllers 8 max.)

- Jumper plug specifies the controller numbers in using multiple controllers (8 mx.) with one host.
- Jumper plug must be set onto each controller according to the controller number.



JP1

Figure 4

NOTES 1) Factory installation: DBO

2) When multiple controllers are used, the terminator (registor pack) must be installed only on the last board. Fig. 5 shows two operating setups; (1) using one controller and (2) using two controllers.

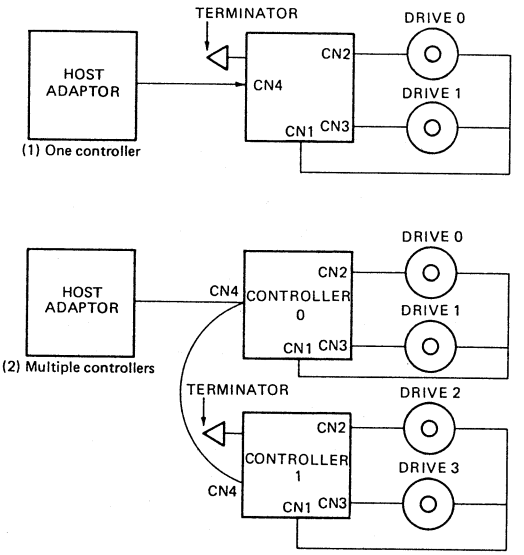


Figure 5

3. OPERATION THEORIES

3.1 Host I/F Signals

(1) Host I/F Connector

2 – $\overline{DB0}$
4 – $\overline{DB1}$
6 – $\overline{DB2}$
8 – $\overline{DB3}$
10 – $\overline{DB4}$
12 – $\overline{DB5}$
14 – $\overline{DB6}$
16 – $\overline{DB7}$
36 – $\overline{BSY}$
38 – $\overline{ACK}$
40 – $\overline{RST}$
42 – $\overline{MSG}$
44 – $\overline{SEL}$
46 – $\overline{C/D}$
48 – $\overline{REQ}$
50 – $\overline{I/O}$

20 ~ 34 – NC
ODD No. – GND

(2) Signal Definitions

- $\overline{DB0} \sim \overline{7}$ (Host ⟷)

  Eight data bits (lines) of the host bus

- $\overline{BSY}$ (Host ⟵)

  The controller generates this active low signal (BUSY) in response to $\overline{SEL}$ and the address bit ($\overline{DB0} \sim 7$) from the host adaptor. This signal informs the host that the controller is ready to conduct transactions on the host bus.

- $\overline{ACK}$ (Host ⟶)

  The host adaptor generates this active low signal (Acknowledge) in response to $\overline{REQ}$ from the controller when the host is ready to receive or transmit a byte of data.

- $\overline{RST}$ (Host ⟶)

  The host adaptor sends this active low signal (Reset) to the controller to force the controller to the idle state. After $\overline{RST}$ has become active, any controller status is cleared. $\overline{RST}$ causes the deactivation of all signals to the drive.

  (NOTE: If this signal is sent while in writing, the data written shall not be warranted.)

- $\overline{MSG}$ (Host ⟵)

  The controller sends this active low signal (Message) to the host adaptor to indicate that the current command has been completed. This sianal is qualified by $\overline{REQ}$.

- $\overline{SEL}$ (Host ⟶)

  The host adaptor sends this active low signal (Select) to initiate a command transaction.

- $\overline{C}/D$ (Host ⟵)

  This signal line (Command/Data) indicates whether the information on the data bus consists of command or data bytes. A low signal means command bytes; a high means data bytes. This signal is qualified by $\overline{REQ}$.

- $\overline{REQ}$ (Host ⟵)

  The controller sends this active low signal to the host adaptor for each byte transferred across the interface. This signal qualifies signals $\overline{I}/O$, $\overline{C}/D$ and $\overline{MSG}$.

- $\overline{I}/O$ (Host ⟵)

  The controller drives this line. A low level on this line indicates that the controller is driving the data in on the host bus, while a high level indicates that the host adaptor is driving the data out on the host bus. The host adaptor monitors this line and use it to enable and disable its data bus drivers. This signal is qualified by $\overline{REQ}$.

(3) Host Bus Status Signals

$\overline{I/O}$	$\overline{C/D}$	$\overline{MSG}$	Definition
High	Low	High	The controller receives command from the host adaptor.
High	High	High	The controller receives data from the host adaptor.
Low	High	High	The controller sends data to the host adaptor.
Low	Low	High	The controller sends error status byte to the host adaptor.
Low	Low	Low	The controller informs the host adaptor that it has completed the current command.

Table 2

3.2 Disk Connectors

(1) Control Signals – CN1 –

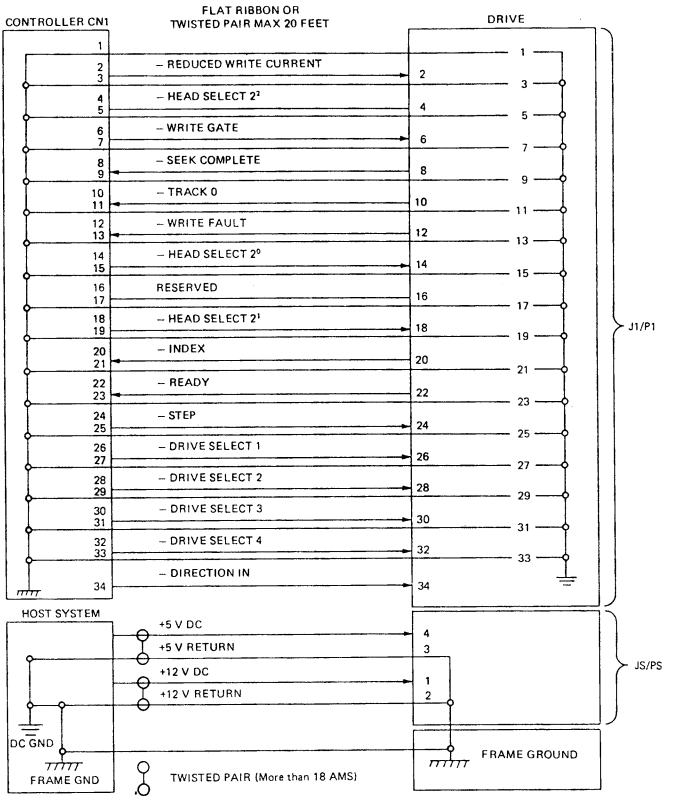


Figure 6

(2) Data Signals –CN2, CN3–

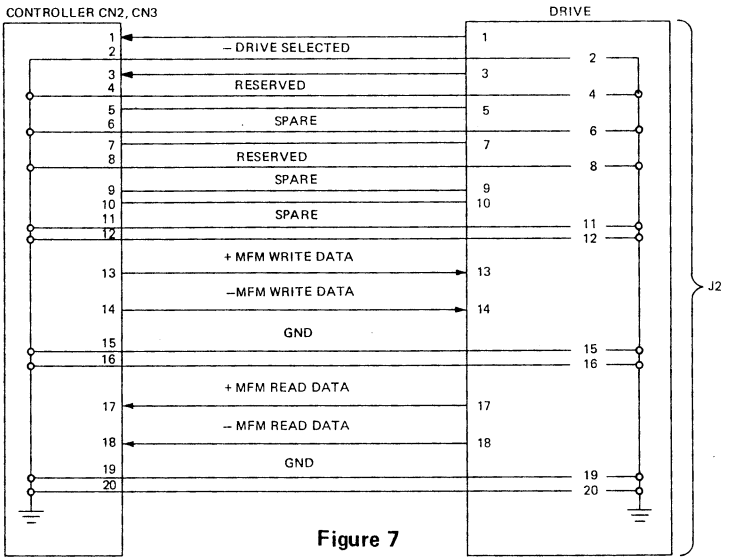


Figure 7

(3) Power Supply –CN5–

4 – +5 V
3 – GND
2 – N.C.
1 – N.C.

3.3 Timing

(1) Select

- The host adaptor must select the controller, before it begins a transaction. The host adaptor selects the controller by activating $\overline{SEL}$ and the address bit of the controller.
- Fig. 8 shows basic timing requirements. Upon receiving both $\overline{SEL}$ and $\overline{DB0}$, the controller activiates $\overline{BSY}$. During the selection process the host controls the data bus as signified by deactivation of $\overline{I/O}$. Selection is completed when $\overline{BSY}$ becomes active. $\overline{SEL}$ must be deactivated by the host interface before the current controller operation has completed.

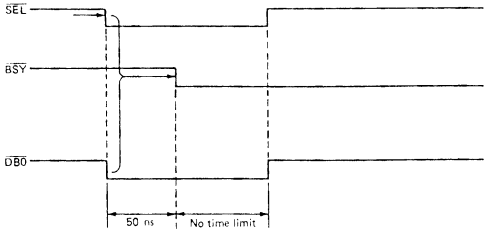


Figure 8

(2) Data Transfer

(2-1) Data Transfer to Host (Data Read)

- Fig. 9 illustrates the required timing for data transfer to Host.

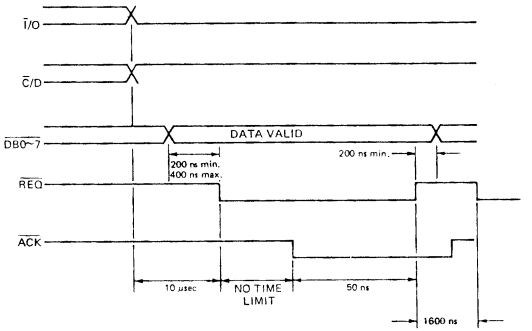


Figure 9

(2-2) Data Transfer from Host (Data Write)

- Fig. 10 illustrates the timing requirements for data transfer from Host.

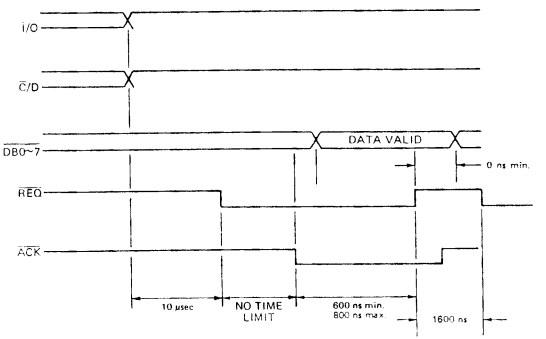


Figure 10

3.4 Track Format

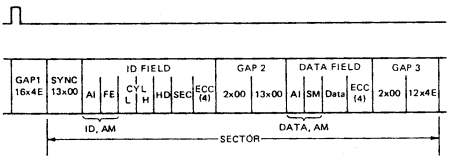


Figure 11

SYNC:	[00] $_{16}$	13 bytes	
ID. AM:	[A1] $_{16}$	1 byte	
	[FC] $_{16}$	1 byte	128 B/S *1
	[FD] $_{16}$		256 B/S
	[FE] $_{16}$		512 B/S
	[FF] $_{16}$		1024 B/S
CYL-L:	[00 ~ FF] $_{16}$	1 byte	
CYL-H:	[00 ~ FF] $_{16}$	1 byte	
HEAD:	[00 ~ 07] $_{16}$	1 byte	
SEC:	[00 ~ 35] $_{16}$	1 byte	
ECC:	[XX] $_{16}$	4 bytes	
GAP2:	[00] $_{16}$	15 bytes	
DATA. AM:	[A1] [SM] $_{16}$ *2	2 bytes	
DATA:	[XX] $_{16}$		
ECC:	[XX] $_{16}$	4 bytes	
GAP3:	[00] $_{16}$	2 bytes	
	[4E] $_{16}$	12 bytes (42 bytes for 512B and 1024B)	
	Total	58 bytes + data length	

*1 B/S = BYTES/SECTOR
*2 SM = SECTOR MARK

3.5 Commands

(1) Device Control Block (DCB) Format

The host sends a six-byte block to the controller to specify the operation. This block is the Device Control Block (DCB). Fig. 12 shows the composition of DCB.

Bit	7	6	5	4	3	2	1	0	
Byte 0	Cmd class			Opcode					DCB
Byte 1	LUN			High Address					
Byte 2	Middle Address								
Byte 3	Low Address								
Byte 4	Interleave or Block Count								
Byte 5	Control Field								

Figure 12

- BYTE 0:
  (Cmd class) Bits 7, 6 and 5 identify the class of command.
  (Opcode) Bits 4 through 0 contain the opcode of command.
- BYTE 1:
  (LUN) Bits 7, 6 and 5 identify the logical unit number of drive.
  (High Address) Bits 4 through 0 contain 21-bit logical disk address 2.
- BYTE 2: Bits 7 through 0 contain 21-bit logical disk.
  (Middle Address) address 1.
- BYTE 3: Bits 7 through 0 contain 21-bit logical disk.
  (Low Address) address 0.
- BYTE 4:
  (Block Count) To specify how many sectors should be formatted.
  or '1': one sector, '0': 256 sectors max.
  (Interleave) To assign sector numbers in formatting.
  1 ~ 53: (128 B/S)
  1 ~ 35: (256 B/S)
  1 ~ 8: (1024 B/S)
  Ex. 256 B/S • Interleave 4

TRACK

0	8	10	18	1	9	11	19	2	A	12	1A	3	B	13	1B	4	C	14	10	5	D	15	1D	6	E	16	1E	7	F	17	1F

• BYTE 5: (Control Field)

This byte allows the user to select options for several different types and makes of disk drives.

The following defines the bits of control byte.

[CONTROL BYTE]

R	E	F	O	S	S	S	S

R: 0 = Retry

1 = No retry

E: 0 = When ECC error is detected, retry will be executed first. If the error is not recovered by Retry, ECC will be execuetd, if possible, to correct the error. The corrected data should be transferred before the command is complete.

1 = ECC shall be directly executed without retry.

F: 0 = Data will be written in (6C) H.

1 = Data in buffers will be written.

S: STEP RATES

S	S	S	S	
0	0	0	0	..... 3 ms
0	0	0	1	..... Seagate ST506
0	0	1	0	..... Tandon
0	1	0	0	..... 200 μs
0	1	0	1	..... 70 μs
0	1	1	0	..... 30 μs
0	1	1	1	..... 15 μs
1	0	0	0	..... 2 ms
1	0	0	1	..... 1.1 ms
1	0	1	0	} Not used
1	1	1	1	

• At the end of command, the controller returns two completion status bytes to the host. Fig. 12-(a) and -(b) show formats of these bytes.

[STATUS – Next to Last Status Byte]

bit	7	6	5	4	3	2	1	0
	0	0	d	0	0	0	E	0

Fig. 12-(a)

Bit 1 (E) indicates whether error cocurred or not.

Bit 5 (d) specifies logical unit number of drive, d = 0 or 1.

[MESSAGE – Last Status Byte]

bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0

Fig. 12-(b)

This status (Message) informs completion of one cycle.

(2) Test Drive Ready (Class 0, Opcode 00)

This command selects a particular drive and verified that the drive is ready.

d = drive, 0 or 1

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	0	0
Byte 1	0	0	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

(3) Recalibrate (Class 0, Opcode 01)

This command positions the read/write (R/W) arm to track 00.

d = drive, 0 or 1

r = retries S = Step Option

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	0	1
Byte 1	0	0	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	r	0	0	0	S	S	S	S

(4) Request Sense Status (Class 0, Opcode 03)

The host must send this command immediately after it detects an error. The command causes the controller to return four bytes of drive and controller status. When an error occurs on a multiple sector data transfer, (read or write), the Request Sense Status command returns the logical address of the failing sector in bytes 1, 2 and 3. If the Request Sense Status command is issued after any of the Format commands or the Check Track Format command, then the logical address returned by the controller points to one sector beyond the last track formatted or checked if there was no error. If there was an error, then the logical address returned points to the track in error.

d = drive, Ø or 1

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	1	1
Byte 1	0	0	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

Bit	7	6	5	4	3	2	1	0
Byte 0	ERROR CODE							
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							

* A summary of ERROR CODE

Error Code (hex)	Meaning
00	No error detected (command completed ok)
01	No index detected from disk drive.
02	No seek complete from disk drive.
03	Write fault from disk drive.
04	Drive not ready after it was selected.
05	Not used.
06	Track 00 not found.
07-0F	Not used.

08 . . . . . Disk drive still seeking.
10 . . . . . ID field read error.
11 . . . . . Uncorrectable data error.
12 . . . . . Address mark not found.
13 . . . . . Not used.
14 . . . . . Target sector not found.
15 . . . . . Seek error.
16-17 . . . . . Not used.
18 . . . . . Correctable data error.
19 . . . . . Bad track flag detected.
1A . . . . . Format error.
1B-1F . . . . . Not used.
20 . . . . . Invalid command.
21 . . . . . Illegal disk address.
22-2F . . . . . Not used.
30 . . . . . RAM diagnostic failure
31 . . . . . Program memory checksum error.
32 . . . . . ECC diagnostic failure.
33-3F . . . . . Not used.

(5) Format Drive (Class 0, Opcode 04)

This command format all sectors with ID and data fields according to the selected interleave factor. The starting address is passed in the DCB. The controller will format from the starting address to the end of the disk.

d = drive, 0 or 1
r = retries
s = Step Option

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	F	0	S	S	S	S

INTERLEAVE (BYTE 4)
128: 1H ~ 35H
256: 01H ~ 1FH
512: 01H ~ 10H
1024: 01H ~ 08H
(F: F = 1, to write data held in buffers into data fields.
F - 0, to write 6C Hex into data fields.)

(6) Check Track Format (Class 0, Opcode 05)

This command checks the format on the specified track for correct ID and interleave. The command does not read the data field.

d = drive, 0 or 1
r = retries
S = Step Option

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	1
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	0	0	S	S	S	S

As for Interleave, refer to (5).

(7) Format Track (Class 0, Opcode 06)

This command formats a specified track and can be used to clear bad-sector flag in all sectors on the specified track that was previously formatted with Format Bad Track command. The command writes 6C Hex into all data fields.

d = drive, 0 or 1
r = retries
S = Step Option

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	F	0	S	S	S	S

As for Interleave, refer to (5).

(8) Format Bad Track (Class 0, Opcode 07)

This command formats the specified track and sets the bad-sector flag in the ID fields. It does not write the data fields.

d = drive, 0 or 1
r = retries
S = Step Option

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	0	0	S	S	S	S

(9) Read (Class 0, Opcode 08)

This command reads the specified number of sectors, starting with the initial sector address contained in the DCB.

d = drive, 0 or 1
r = retries
E = retry option on data ECC error
S = Step Option

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	0	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	Block Count							
Byte 5	r	E	0	0	S	S	S	S

(10) Write (Class 0, Opcode 0A)

This command writes the specified number of sectors, starting with the initial sector address contained in the DCB.

d = drive, 0 or 1
r = retries
S - Step Option

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	1	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	Block Count							
Byte 5	r	0	0	0	S	S	S	S

(11) Seek (Class 0, Opcode 0B)

This command initiates a seek to the track specified in the DCB and check ID fields. If this command is executed in buffer mode, if sends only step-pulse.

d = drive, 0 or 1
r = retries
S = Step Option

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	1	1
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	/	/	/	/	/	/	/	/
Byte 5	r	0	0	0	S	S	S	S

(12) Initialize Drive Characteristics (Class 0, Opcode 0C)

This command enables the user to configure the controller to work with drives that have different capacities and characteristics. However, both drive 0 and drive 1 must be of the same manufacturer and model.

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	0	0
Byte 1	/	/	/	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Type 5	/	/	/	/	/	/	/	/

Parameter Bytes

After the host sends the command (DCB) to the controller, it then sends an eight-byte block of data that contains the drive parameters. The eight bytes are listed as follows:

Bit	7	6	5	4	3	2	1	0	
Byte 0	C	C	C	C	C	C	C	C	.... Max. cylinder address (High)
Byte 1	C	C	C	C	C	C	C	C	.... Max. cylinder address (Low)
Byte 2	0	0	0	0	H	H	H	H	.... Max. head number
Byte 3	W	W	W	W	W	W	W	W	.... Starting reduced write current cylinder (High)
Byte 4	W	W	W	W	W	W	W	W	.... Starting reduced write current cylinder (Low)
Byte 5	P	P	P	P	P	P	P	P	.... Starting write precompesation cylinder (High)
Byte 6	P	P	P	P	P	P	P	P	.... Starting write precompensation cylinder (Low)
Byte 7	0	0	0	0	E	E	E	E	.... Max. ECC data burst length

(Ex.)

Bit	7	6	5	4	3	2	1	0	
Byte 0	0	0	0	0	0	0	0	0	0099Hx
Byte 1	1	0	0	1	1	0	0	1	
Byte 2	0	0	0	0	0	1	0	0	4Hx
Byte 3	0	0	0	0	0	0	0	0	0080Hx
Byte 4	1	0	0	0	0	0	0	0	
Byte 5	0	0	0	0	0	0	0	0	0000Hx
Byte 6	0	0	0	0	0	0	0	0	
Byte 7	0	0	0	0	1	0	1	1	0BHx

(13) Read ECC Burst Error Length (Class 0, Opcode 0D)

This command transfers one byte to the host. This byte contains the value of the ECC burst length that controller detected during the last Read command. This byte is valid only after a correctable ECC data error, type 1, code 8.

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	0	1
Byte 1	/	/	/	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

(14) RAM Diagnostic (Class 7, Opcode 00)

This command executes a data pattern test on the RAM buffer.

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	0	0	0
Byte 1	/	/	/	/	/	/	/	/
Btye 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

(15) Drive Daignostic (Class 7, Opcode 03)

This command tests both the drive and the drive-to-controller interface. The controller sends recalibrate and seek commands to the selected drive and verifies sector 0 of all the tracks on the disk. The controller does not execute any write operations during this command.

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	0	1	1
Byte 1	0	0	d	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	r	0	0	0	S	S	S	S

(16) Controller Internal Diagnostics (Class 7, Opcode 04)

This command causes the controller to execute a self-test. The controller checks its internal processor, data buffers, ECC circuity, and the checksum of the program memory. The controller does not access the drive.

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	0	0
Byte 1	/	/	/	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

(17) Read Long (Class 7, Opcode 05)

This command transfers the target sector and four bytes of data ECC to the host. If an ECC error occurs during the read, the controller does not attempt to correct the data field. This command is useful in recovering data from a sector that contains an uncorrectable ECC error. It is also useful during diagnostic operations.

d = drive, 0 or 1
r = retries
S = Step Option

Bit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	0	1
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	Block Count							
Byte 5	r	0	0	0	S	S	S	S

(18) Write Long (Class 7, Opcode 06)

This command transfers a sector of data and four appended ECC bytes to the drive. During this operation, the host supplies the four ECC bytes instead of the usual hardware-generated ECC bytes. This is useful only for diagnostic operations.

d = drive, 0 or 1
r = retries
S = Step Option

Vit	7	6	5	4	3	2	1	0
Byte 0	1	1	1	0	0	1	1	0
Byte 1	0	0	d	High Address				
Byte 2	Middle Address							
Byte 3	Low Address							
Byte 4	Block Count							
Byte 5	r	0	0	0	S	S	S	S

(19) Format Alternate Track (Class 0, Opcode E)

Format Alternate Track will format the header fields of the Bad Track with the alternate track information (assigned by the host). The alternate track is formatted to identify it as an laternate.

Command Bytes
d = drive, 0 or 1
r = retries
S = Step Option

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	1	0
Byte 1	0	0	d	Logical Address Hi				
Byte 2	Logical Address Middle							
Byte 3	Logical Address Low							
Byte 4	0	0	0	Interleave				
Byte 5	r	0	F	0	S	S	S	S

- The logical address in the command bytes point to the 'Bad Track'. Sector address is ignored, defaulting to sector 0.
- The interleave byte (4) is programmed the same as in the format command, and is used on the alternate track.
- If Bit 5 of Control Byte (5) is set, the data in the existing sector buffer is used to fill the data field. If not set, the data field is written with 6C Hex.
- After issuing the command the controller will ask for 3 bytes. These bytes points to the host assigned alternate logical address. Sector address is ignored.

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	Logical Address Hi				
Byte 1	Logical Address Middle							
Byte 2	Logical Address Low							

• After receiving the command and the assigned alternate, the controller perform the following:

1) Seeks to 'Alternate Assigned Track' and verifies that it is not already an assigned alternate track, flagged bad track.
   (If the track has already been assigned as an alternate or is flagged 'BAD', then error code 1D Hex is given, and the command is aborted. This usually implies that the host is attempting to assign two bad tracks to the same alternate track.)
2) Formats the track as an assigned alternate track.
3) Seeks to the 'Bad Track' and formats the header as a spare track pointing to the assigned alternate.

(20) Write Sector Buffer (Class 0, Opcode 0F)

Used to fill the sector buffer with a host given data pattern. No transfer of data takes place between the drive and the controller.

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	1	1
Byte 1	/	/	/	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

(21) Read Sector Buffer (Class 0, Opcode 10)

This command sends the data (depending on sector size jumper) to the host from the sector buffer.

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	1	0	0	0	0
Byte 1	/	/	/	/	/	/	/	/
Byte 2	/	/	/	/	/	/	/	/
Byte 3	/	/	/	/	/	/	/	/
Byte 4	/	/	/	/	/	/	/	/
Byte 5	/	/	/	/	/	/	/	/

3.6 Execution of Diagnostics

Since all of the diagnostics are not executed by the controller on power up, it is suggested that they be envoked by the host in the following order:

1) Controller internal diagnostics (Command code E4)
   This diagnostic tests all the logical and decision making capability of the controller as well as the program memory checksum and the error detection and correction circuits (ECC). Execution of this diagnostic ensures that the contoller can communicate with the host.
2) Ram Diagnostic (Command code E0) should be executed next. This command verifies that the sector buffer is operational by writing, reading and vaerifying various data patterns to and from all locations.
3) If the parameters of the connected drives are different than the default parameters, see Paragraph 3.5.(12), the new configuration must be sent to the controller using the Initialize Drive Characteristics command (Command code 0C) before the Drive Diagnostic is executed.
4) Before the Drive Diagnostic is executed, the host program should continuously issue a Test Drive Ready command to the controller (Command code 00) with the papropriate time-out until the drive becomes ready.
5) Drive Diagnostic (Command code E3). This diagnostic issues a Recalibrate to the disk drive and then steps through all tracks veryfingi the ECC on the ID fields of the first sector of each track. If this diagnostic passes, it implies that the disk has been formatted and that the first ID fields of each tarck is good.

4. OPERATIONS

4.1 Formatting

- Drive characteristics (Ex.)
  1) Cylinder: 153 max.
  2) Head: 4 mx.
  3) Reduced write current: at 128 cylinder
  4) Write precompensation: 64
  5) ECC data burst length: 11 bits max.
- Alternate is provided by Command 0C in power-on or reset.
- Format Drive Command 04 executes formatting up to the maximum cylinder. Starting track begins from logical sector of the command.
- When logical address is altrenated to physical address sector address should be ignored.
- In formatting all over the drive, logical sector should be 0. Formatting is specified with dip-switches (See Fig. 3 & Table 1, P.5).

- When an error occurs in formatting, formatting will be stopped at the track and error status repeated. Its status is indicated by request sense status.
- Format track 06 is used to format one track. A tarck specified by command will be sought and formatted.
- Command 07 is used to register a bad track. A track registered as bad track cannot be accessed.
- Command 0E is used to format an alternate track. (See 3.5.(19) for details).

4.2 Data Read/Write

- After receiving command, the controller will seeks to the specified sector and write/read the block count. Block count starts from (01)H through (00)H-256 blocks.
- When an error occurs, the aadress will stop.
- Correctable error in reading
  Corrected data will be transferred and Read will complete. In this case, ECC error length will be detected by executing Read ECC Burst Error Length command.
- Uncorrectable error in reading
  Data will not be transferred and Reaad will complete.

4.3 Over-Lap Seek

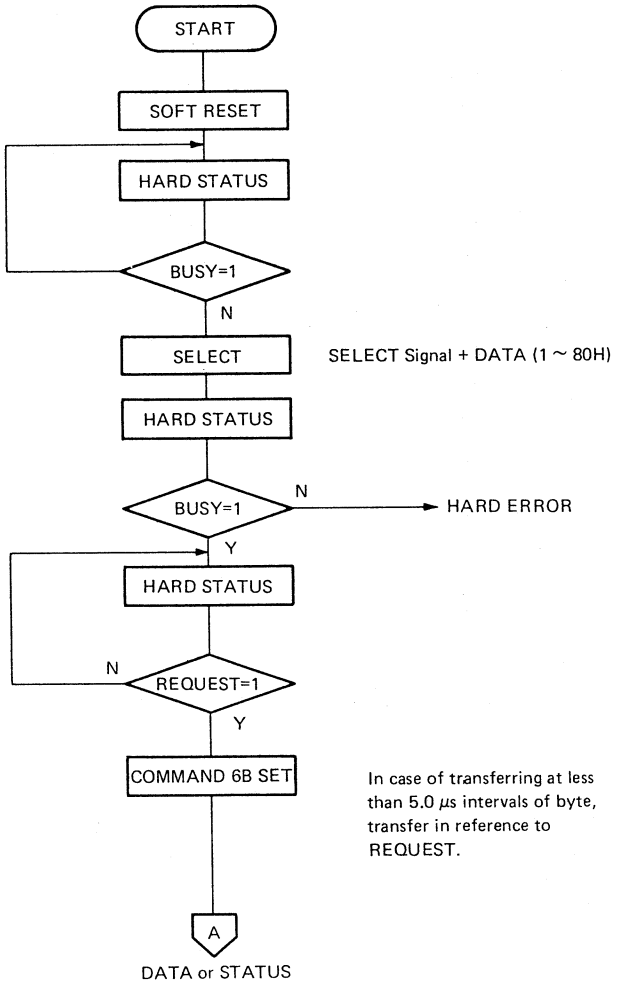
Since drives employ buffered seeks, seek commands can be overlapped. The Test Drive Ready command can be used with overlapped seeks to determine when a drive has completed seeking before issuing the next command. If the drive is tsill seeking, the status byte at the end of the command will indicate an error, and the sense status will indicate 'diver still seeikng' (type 0 error, code 8). A sequence of Test Drive Ready commands can thus be used to determine when the drive is ready for the next command. There is no timeout condition in the controller, waiting for the buffered step seeks to complete.

Operational Ex.

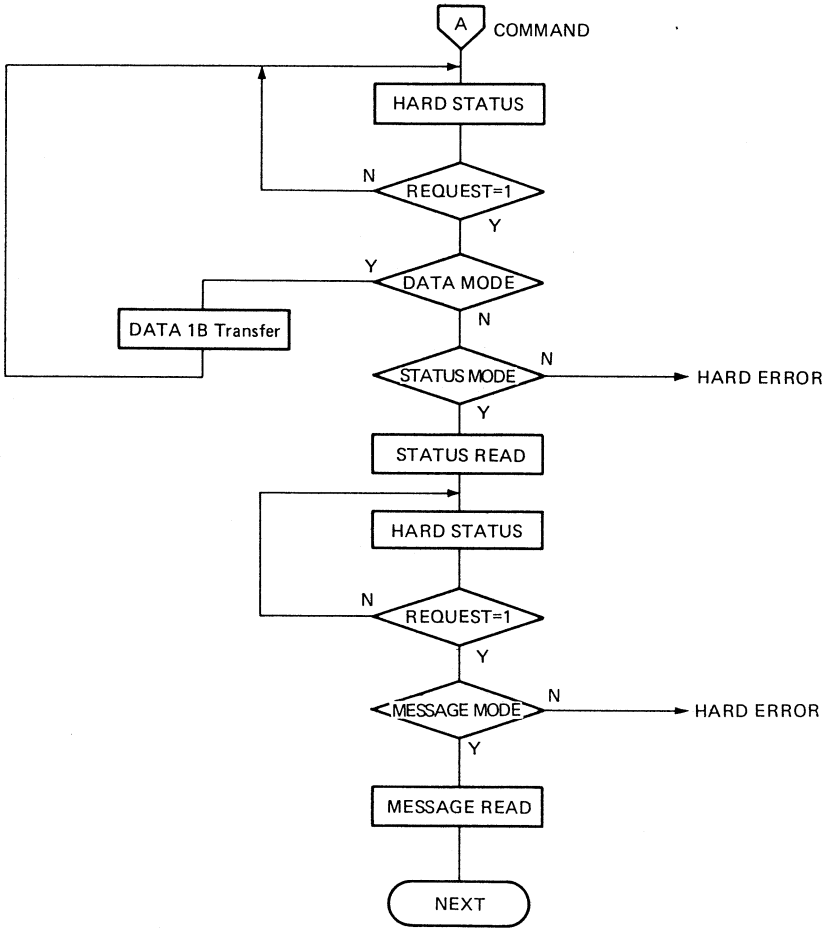
1) Drive 0 Seek Command (buffered step seek) } overlapped
2) Drive 1 Read Command }
3) Drive 2 Read Command (read after seek completes)

5. OPERATIONAL FLOW CHART

5.1 Select and Command Transfers



5.2 Data Transfer or Status Read



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