

# MICOM INDUSTRIES INC.

ELECTRONIC CONSULTANTS

3996 DUNDAS STREET, BURNABY, B.C. V5C 1A5

TELEPHONE 294-5692

## 64 K DYNAMIC RAM BOARD FOR THE SS-50 OR SS-50C BUS

- Economical
- Reliable
- On board refresh circuitry (looks like static ram to processor)
- Low current drain (less than 1 amp)
- Any 8 K segment may be selected or de-selected via DIP switch
- can decode 20 address lines

Assemble board as per layout diagram.

If extended addressing is required, insert jumper at location J. For 16 address lines the jumper is left off and, optionally the 74LS136, the 4 DIP switch and R<sup>10</sup> to R<sup>13</sup> may also be left off. For extended addressing the 4 DIP switch is used as a hexadecimal page selector. Close switches for 0, open for 1. For example for page 0 all switches must be closed, for page F all must be open: page 6 would be: ~~on~~ off ~~off~~ on etc.

The 8 DIP switch is used to deselect one or more 8 K segments within the 64 K address space. Open switch to de-select. For instance if your board sits at page 0 and your monitor ROM and I/O are at E000 and up, open switch E to give you space from E000 to FFFF.

\* NOTE PIN 1 ON RAM CHIPS INVERTED  
FROM THE REST!

MICOM INDUSTRIES INC.  
64 K DYNAMIC RAM BOARD

PARTS LIST

QUANTITY

DESCRIPTION

CAPACITORS

<del>2</del>	<del>100 pfd polystyrene</del>
<del>1</del>	<del>110 " "</del>
8	0.1 ufd Disc ceramic or tantalum
1	220 ufd 16 V. Electrolytic

RESISTORS

	<del>3.3K 1/4W</del>
6	<del>1.0 K ohm 1/4 w 5%</del>
<del>2</del>	<del>4.7 K " " "</del>
<del>1</del>	<del>5.6 K " " "</del>
1	3.3 K ohm 8 resistor DIP pack (or 8 individual resistors)

INTEGRATED CIRCUITS

1	74LS00
1	74LS02
1	74LS30
1	74LS42
1	74LS74
1	74LS136 *
4	74LS157
1	74LS393
8	MB8264 (FUJITSU) or MCM6664 (MOTOROLA)
2	DM8835
1	9602
1	7805 Voltage Regulator

MISCELLANEOUS

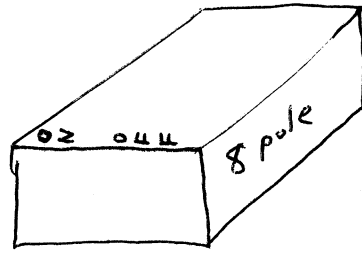
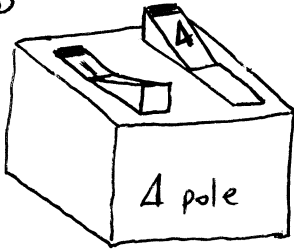
1	4 Position DIP Switch *
1	8 " " "
5	Molex 09-52-3101 10 Pin Female Connector
1	TO-220 Heat sink

\* ONLY NEEDED FOR EXTENDED ADDRESSING (20 LINES)

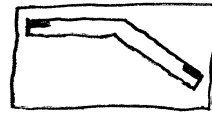
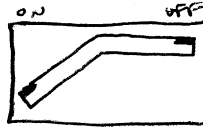
(See spec)

1  
closed  
GND

$\neq \emptyset$   
open  
+5



ON  
select  
closed

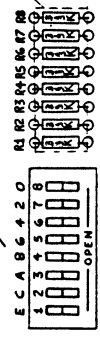


OFF open deselect

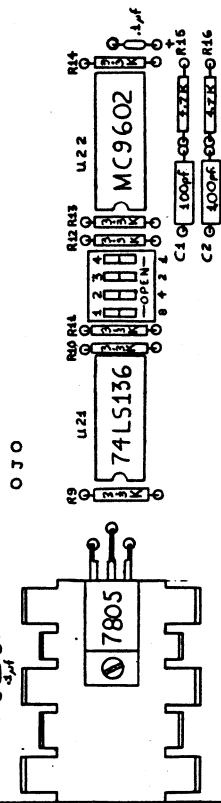
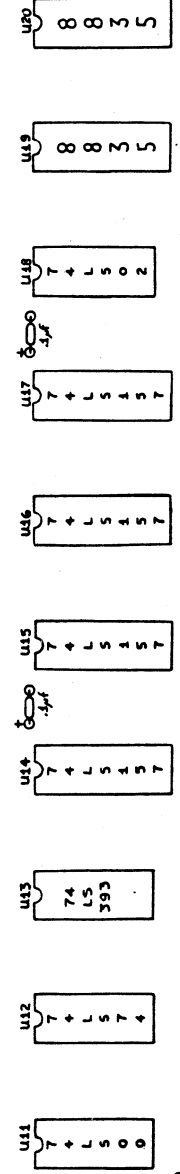
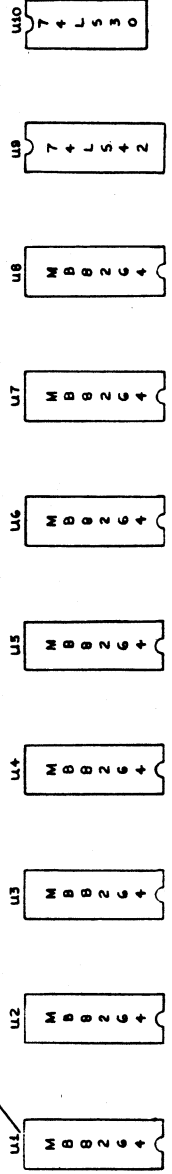
but DIP switch numbers 1-8  
on schematic are backwards

RESISTORS OR DIP

OPEN TO DESELECT



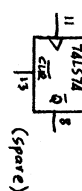
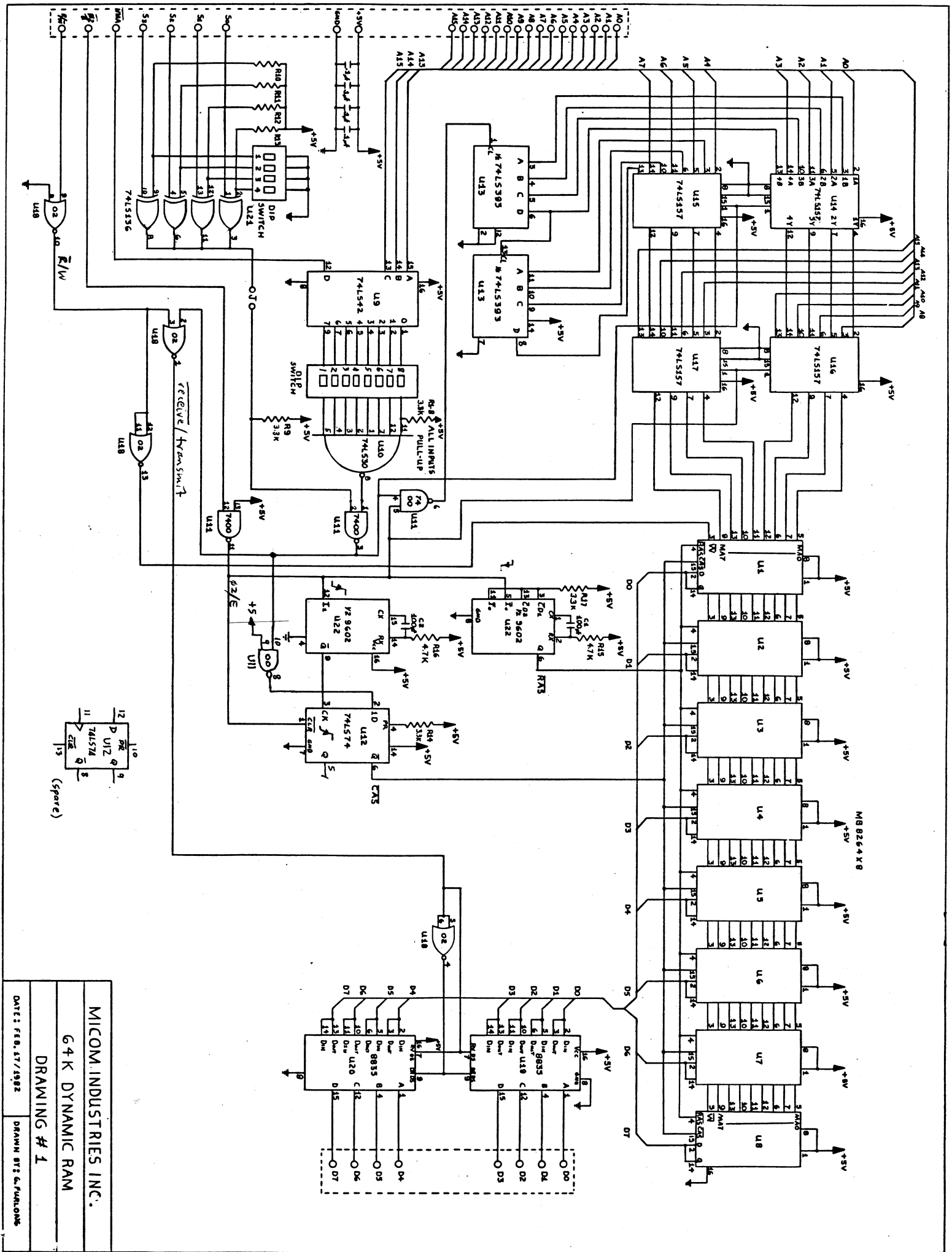
NOTE: RANS ARE UPSIDE-DOWN



220pF

C1 = 68pF  
C2 = 0pF

MICOM INDUSTRIES INC.
64 K RAM PCB LAYOUT
DRAWING #2
FEB. 15/82
NO SCALE



MICROM INDUSTRIES INC.

64K DYNAMIC RAM

DRAWING # 1

DATE: FEB. 27/1982

DRAWN BY: G.P./R/ONS

64K DRAM Board for SS-50 Bus from Micom Industries Inc.

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The printed circuit board and the documentation, as supplied, have several errors. In addition, there are a few simple enhancements to the original design that can be made. The items below are not necessarily in the sequence in which you will perform them. In particular, you should look at all the steps and do all the necessary trace cutting before you start installing any parts on the board.

- 1) If you plan on using extended addressing, you need to fix a mistake on the circuit board and the schematics. If you will not be using extended addressing (and will leave the jumper at "J" open), then you do not need to make these changes:
  - a) cut the trace (on the solder side) between U11 pin 1 and U12 pin 2
  - b) install a jumper wire between U11 pins 3 and 10
  - c) install a jumper wire between U11 pins 9 and 14
  - d) install a jumper wire between U11 pin 8 and U12 pin 2
- 2) If there is any chance that you will be using DRAMs that have a 256 cycle refresh (TMS4164 from Texas Instruments, or 256K DRAMs), you need to modify the circuit board and schematics. If you will only be using DRAMs that have a 128 cycle refresh, you do not need to make these changes:
  - a) cut the trace (component side) between U15 pin 13 and ground
  - b) install a jumper wire between U13 pin 8 and U15 pin 13
- 3) Although many engineers may consider the number of bypass capacitors on the board to be sufficient, I would suggest adding another .1 uF cap between pins 7 and 14 of U12, and another four caps between pins 8 and 16 of every other DRAM chip.
- 4) Although unconnected input pins of 74LSxx parts tend to float to a logic "1", connecting them to a solid logic "0" or "1" source is better. You may wish to install a jumper wire between U12 pins 7 and 11 and another one between U12 pins 7 and 13.
- 5) The schematics show the 74LS136 to have inverting outputs (they have "bubbles" drawn on the output pins). This is wrong, and the schematics should have the "bubbles" removed. **But the outputs are open collectors.**
- 6) The schematics show the 8 position DIP switch numbered from 1 at the top to 8 at the bottom. This is backwards, and the schematics should be changed to number the DIP switch with switch 1 at the bottom and switch 8 at the top. The parts placement diagram is correct.
- 7) The board is not designed to properly allow switching back and forth between 1 MHz and 2 MHz as the values of capacitors C1 and C2 fix the speed of the board. However, if you build the board for 2 MHz operation, and you have a 2 MHz 6809 uF installed, the board will probably work at 1 MHz as well as 2 MHz.

	1 MHz	2 MHz
	-----	-----
C1	100 pF	68 pF
C2	100 pF	0 pF

8) The top half of the parts list should read as follows:

CAPACITORS

- 2 100 pF polystyrene (for 1 MHz only operation)
- 1 68 pF polystyrene (for 2 MHz operation)
- 8 0.1 uF disk ceramic or monolithic (add 5 more if step #3 done)
- 1 220 uF 16 volt electrolytic

RESISTORS

- 6 3.3K 1/4 watt 5%
- 2 4.7K 1/4 watt 5%
- 1 3.3K ohm 16 pin resistor DIP - 8 separate resistors  
(or 8 individual 3.3K 1/4 watt resistors)

- 9) The documentation states that if extended addressing is not used, that resistors "R10 to R15" may be left off. This should read "R10 to R13".
- 10) The documentation describing how to set the 4 position DIP switch is wrong -- all occurrences of "open" should be changed to "closed", and vice versa. The corrected version would read: "Open switches for 0, close for 1. For example, for page 0 all switches must be open, for page F all must be closed; page 6 would be: off on on off, etc."
- 11) Be very careful when installing the DRAM chips, as they are installed upside down compared to all the other chips on the board; that is, the DRAM chips have the pin 1 end facing the bottom of the board where all the other chips have pin 1 facing the top of the board. Refer to the parts placement drawing for the correct orientation.
- 12) Although I haven't actually tried it, converting the board to 256K bytes should work. These instructions are not complete, but should get you started:
- a) cut the trace (solder side) between U8 pin 1 and the +5v bus
  - b) cut the traces that connect pins 3 and 11 of U21 to the extended addressing circuitry (or just bend up these two IC pins)
  - c) take an extra 74LS157 chip and carefully bend pins 2,3,4,5,6,7 and pins 9,10,11,12,13,14 up, leaving only pins 1,8,15,16 still pointing down
  - d) place this new chip on top of U17 piggyback style, and solder pins 1, 8, 15, and 16 of the two chips in parallel
  - e) install a jumper wire between pin 12 of this new chip and U7 pin 1
  - f) install a jumper wire between pin 13 of this new chip and U21 pin 3
  - g) install a jumper wire between pin 14 of this new chip and U21 pin 11
  - h) install jumper wires to connect pins 2,3,5,6,8,10,11 of this new chip together (to ground unused input pins)
- 13) If your SS-50 motherboard and CPU board don't use extended addressing to decode the I/O and ROM address spaces, you end up wasting one or two 8K blocks in every 64K page. There is a way to get around this, but at the expense of reducing the maximum memory capacity from 1 Megabyte to only 512K. I haven't tried it yet, but if you swap address lines A15 and S0 (use S2 if the board has been converted to 256K), then set the 4 position DIP switch that selects S0 (or S2 for 256K) appropriately, you will have the board occupy the lower 32K bytes of each of 2 adjacent 64K pages (or 8

pages for 256K board). Since the I/O or ROM address spaces are always somewhere in the upper 32K, no RAM needs to be disabled and wasted.

This document prepared by David C. Wiens of Sardis Technologies. Use the information contained herein at your own risk -- no warranties or guarantees of any kind are offered.

....jdm64k.DW127.881012.1612



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The 8 DIP switch is used to deselect one or more 8 K segments within the 64 K address space. Open switch to de-select. For instance if your board sits at page 0 and your monitor ROM and I/O are at E000 and up, open switch E to give you space from E000 to FFFF.

MICOM INDUSTRIES INC.  
64 K DYNAMIC RAM BOARD PARTS

QUANTITY

DESCRIPTION

CAPACITORS

~~21-68 PF~~ 100 pfd polystyrene  
8 0.1 ufd Disc  
1 220 ufd 16 V. Electrolytic (RADIAL LEADS)

RESISTORS

14 3.3 K ohm 1/4 w 5%  
2 4.7 k " " "

INTEGRATED CIRCUITS

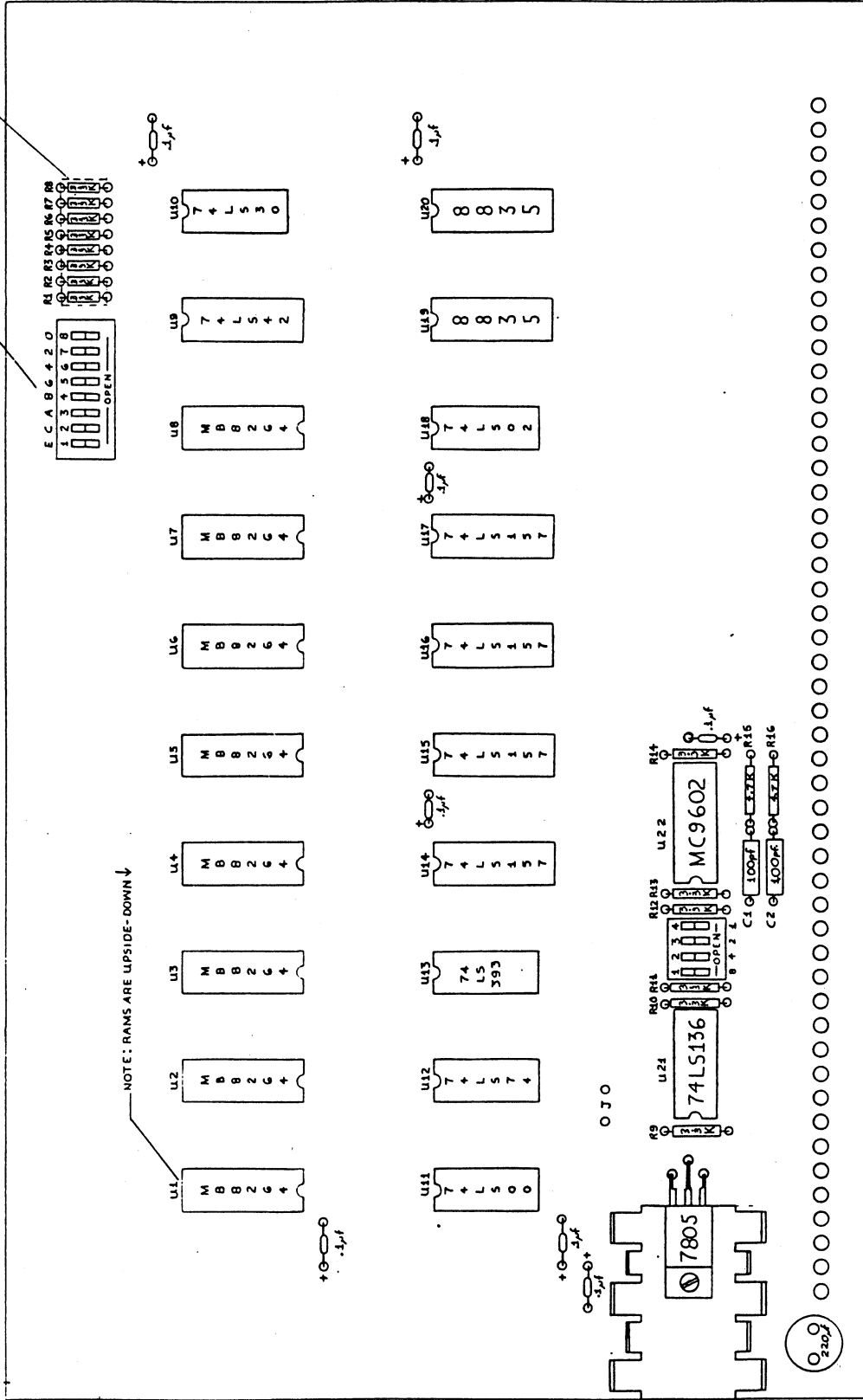
1 74LS00  
1 74LS02  
1 74LS30  
1 74LS42  
1 74LS74  
1 74LS136 \*  
4 74LS157  
1 74LS393  
8 MB8264 or MCM6664  
2 DM8835  
1 9602

MISCELLANEOUS

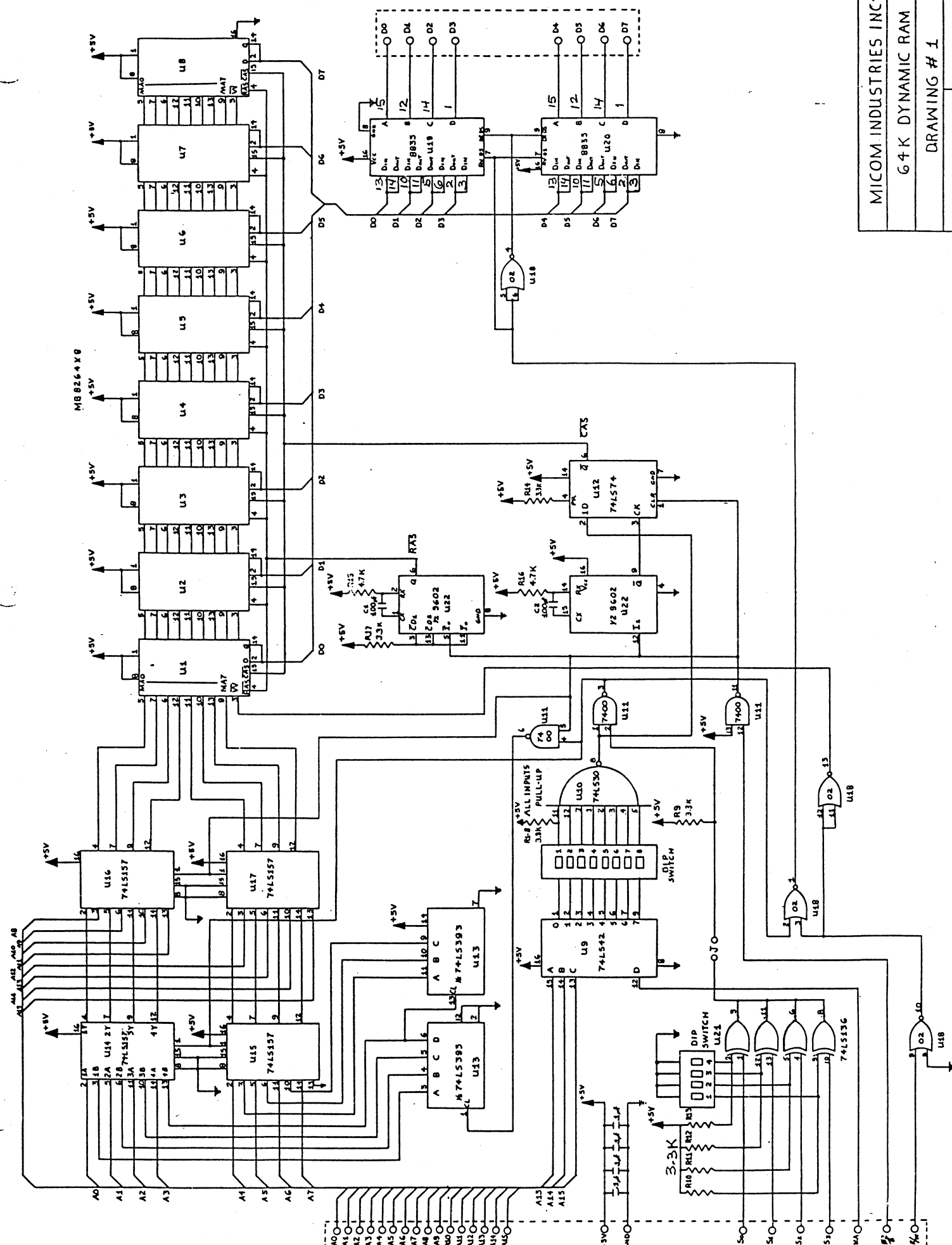
1 4 Position Dip Switch \*  
1 8 " " "  
5 Molex 09-52-3101 10 Pin Female Connector  
1 TO-220 Heat sink

\* - OPTIONAL EXTENDED ADDRESSING FOR 20 ADDRESS LINES

OPEN TO DESELECT  
RESISTORS OR DIP



MICOM INDUSTRIES INC.  
64 K RAM PCB LAYOUT  
DRAWING #2  
FEB. 15/82  
DRAWN BY: S/P/N/12006  
NO SCALE



MB 8264 X 8

MICOM INDUSTRIES INC.  
 64 K DYNAMIC RAM  
 DRAWING # 1  
 DATE: FEB. 27/1982  
 DRAWN BY: G. FURLONG